

# Ground Systems

## PMC Decom/Simulator 30 Mbps, 50 Mbps

**DSZ543, DSZ545**

- Decommutates and simulates a serial PCM data stream from 10 bps to 30 Mbps (DSZ543) or 10 bps to 50 Mbps (DSZ545) to IRIG Class II standards
- Generates standard IRIG data codes including NRZ-L, NRZ-M, NRZ-S
- Simulates telemetry outputs (data and clock) to the rear panel or to any of the 8 internal stream buses on the carrier
- Simulates 1 to 16 major frame formats and switches decom formats per module on operator command or format ID word
- Encodes minor frames (up to 1,024) and subframes
- Aligns MSB or LSB on a word-by-word basis
- Provides independent frame sync and subframe sync data pass qualifiers
- Adds / Checks / Strips parity (odd, even, off) and adds / verifies CRC
- Decom supports data and clock inputs from TTL or RS-422 / LVDS (DSZ543-D, DSZ545-D) sources
- Supports VME Mezzanine Carriers (ZCM596, ZCA596)



The PMC Decommutator / Simulator 30 Mbps (DSZ543) and 50 Mbps (DSZ545) modules are multi-format dynamic PCM test instruments designed for the most robust and demanding Class II telemetry applications. They provide frame-synchronized format switching for up to 16 unique formats and a large aggregate major frame size to over 4 million words, with minor frames to 65,536 words.

Both modules generate a quality status word to report data integrity and offer flexible synchronization strategy, parity checking, and CRC. Module set up is via a GUI common to all system decoms and simulators, and both the GUI and API provide for continuous module status monitoring.

Simulator functions can be used to test the Decommutator to IRIG 106 Class II standards and the database defining the PCM data stream. They provide static and dynamic simulation capabilities for virtually all telemetry formats in both open- and closed-loop applications, including multistage events, simulating complex combinations of computer, sensor, and discrete data. The simulators generate a serial data stream in any selected code at rates up to 50 Mbps and can switch formats at minor and major frame boundaries for up to 16 different formats.

Data sources may be selected dynamically for system checkout and calibration requirements, and data word values may be changed without interrupting the bit stream. Multiple modules can be included in the same system for simulating and decommutating independent data streams.



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# Decommutator

## Decom Inputs

Sources.....	2 TTL Inputs, 1 RS-422 / LVDS Input, 8 LVDS Internal Stream Buses on carrier module
Data Rates .....	10 bits/sec to 50 Mbps
PCM Data Codes .....	NRZ-L
Data Length .....	Variable from 4 to 32 bits per word (min 8 bit average @ 40Mb)
Data Polarity.....	Normal / Inverted / Auto (no Auto with FCC/URC)
Data Alignment.....	MSB / LSB first per word
Parity Check .....	On / Off per word, Odd / Even per word
Parity Location .....	Last bit
Parity Stripping .....	Strip always (if defined)
CRC Checking.....	Any 4 to 32 bit Polynomial, On / Off per word
Input Levels.....	TTL (data / clock), RS-422 / LVDS (data / clock)
Clock Input Phase.....	0, 180 degrees
Clock Duty Cycle.....	50% ± 10%

## Decom Data Pass Qualifiers

Frame Sync .....	Search, check, verify or lock
Subframe Sync .....	Search, check, verify or lock
Parity .....	Pass always or pass if good
CRC .....	Pass always or pass if good
Active Format .....	Pass if format in memory
Parameter .....	Pass if parameter selected for output

## Decom Formats

Format Size: (4-32 bit words)	
Frames per Major Frame.....	Up to 1024 minor frames*
*Subject to words per major frame limits	
1 Format	
Words per Major Frame .....	4 to 4,194,304 (4M)
Words per Minor Frame.....	4 to 65,536 (64K)
2 Formats	
Words per Major Frame .....	4 to 2,097,152 (2M)
Words per Minor Frame.....	4 to 65,536 (64K)
3-4 Formats	
Words per Major Frame .....	4 to 1,048,576 (1M)
Words per Minor Frame.....	4 to 65,536 (64K)
5-8 Formats	
Words per Major Frame .....	4 to 524,228 (512K)
Words per Minor Frame.....	4 to 65,536 (64K)
9-16 Formats	
Words per Major Frame .....	4 to 262,144 (256K)
Words per Minor Frame.....	4 to 65,536 (64K)
Format Switching Control	
Memory Resident Formats.....	Up to 16
Switch Mechanism.....	Switch on Command; Switch on Format ID Word
Format ID Word.....	4 to 10 consecutive bits, fixed bit position in frame
Format Switching Boundary.....	At the beginning of the next word after the format switch word or at the end of the current minor frame
Format Variables .....	Words per minor frame, word locations, bits per word, words per major frame, bits per minor frame
Format Constants.....	Frame sync pattern, sub-frame sync pattern, sub-frame sync method, data polarity, format switch word position, format switch word length

## Decom Frame Sync Characteristics

Frame Sync Pattern Length.....	8 to 64 bits
Search to Lock .....	1 to 16 valid sync words
Lock to Search.....	1 to 16 invalid sync words
Error Threshold.....	0 to 7 bits
Bit Slip Window.....	0 to ± 3 bits

## Decom Subframe Sync Characteristics

Subframe Sync Bits.....	8 to 64 for FCC/URC; 4 to 10 for SFID
SFID Offset .....	0 to 28 Bits
Method .....	SFID, URC, FCC, none
Search to Lock .....	1 to 16 valid sync words
Lock to Search.....	1 to 16 invalid sync words
Error Threshold.....	0 to 7 bits for FCC/URC; 0 for SFID

## Decom Status

Output to MUXbus .....	Frame Sync State, Sub-Frame Sync State, Polarity, Clock Detector, Data Detector, Bit Slip Count, Bit Slip Status, Frame Sync Bit Error Status, Active Format, Valid Format, Input Source, Parity Error Status, CRC Status
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## Other Decom Characteristics

Clock and Data Presence Detector	
Sub-Frame Lock can occur on any Minor Frame or at the start of Major Frame	
Sign Extend or Zero Extend Data to 32 Bits on MUXbus	
Support for defining words by common word location and bit offset in S/W	
Sub-Sub-Frame support using Embedded Processor	



# Simulator

## Basic Features

Data Rates	. . . . .10 bits per second to 50 Mbps
Data Codes	. . . . .IRIG Codes: NRZ-L, NRZ-M, NRZ-S
Clock Source	. . . . .Internal programmable, External
Clock Output Phase	. . . . .0 or 180 degrees
Clock Accuracy	. . . . .0.01% of programmed bit rate (100 ppm)
Clock Duty Cycle	. . . . .50% ± 10%
Data Length	. . . . .4 to 32 bits per word (plus parity if enabled)
Data Polarity	. . . . .Normal or inverted per stream
Data Alignment	. . . . .LSB or MSB first per word
CRC Generation	. . . . .Any 4 to 32 bit Polynomial
CRC Word Inclusion	. . . . .Any Word
Parity Bit Generation	. . . . .None, odd, or even per word
Randomizer	. . . . .Enabled or disabled for all data codes
Randomizer Sequence Length	2 <sup>15</sup> - 1 (per IRIG 106), 2 <sup>11</sup> - 1, 2 <sup>17</sup> - 1

## Data Sources

Static Data	. . . . .Common Word, Frame Sync, Sub-Frame Sync, 1M Static Values
Static Data Word Rate	. . . . .8M Words / Sec
Function Generators	. . . . .Software Defined Functions
Dynamic Data Word Rate	. . . . .8M Words / Sec (with High Performance Option)
MUXbus Data Sources	. . . . .Any 2 to 32 Bit Parameter
MUXbus Data Word Rate	. . . . .8M Words / Sec

## Frame Characteristics

Frame Sync Bits	. . . . .4 to 64
Words per Major Frame	. . . . .4 to 4,096K - 32-bit words (minimum value subject to the maximum word rate and minimum frame sync pattern size limits)
Words per Minor Frame	. . . . .4 to 64K - 32-bit words (subject to the words per major frame limits)
Frames per Major Frame	. . . . .1 to 1,024 (subject to the words per major frame limits)
Super-commutation	. . . . .All data sources into any combination of word locations
Number of Major Frame Formats	. . . . .16
Format Switch Boundary	. . . . .Next Major Frame, Next Minor Frame
Format Switch Mechanism	. . . . .Command, MUXbus Input
Number of Sub-Frames	. . . . .1
Sub-Frame Sync Bits	. . . . .4 to 64
Sub-Frame Sync Methods	. . . . .None, SFID, URC, or FCC

## Outputs

Simulated Telemetry Outputs	Data and clock to the rear panel, or to any of the 8 internal stream buses on the carrier module
Simulated Telemetry Output Levels	TTL (into one TTL load), or RS-422/ LVDS, clock and data, LVDS to internal stream buses
Simulator Status Outputs to MUXbus II	Format Switch, Format Number, Minor Frame Number, FIFO Under- Run Status

## General Requirements

System	550 or Avalon Chassis 1 PMC slot
Rear Panel:	
DCZ TTL Models	. . . . .1 slot, 2 TTL clock and data (2 BNC coaxial);
DSZ TTL Models	. . . . .1 slot, 2 TTL clock and data (4 BNC coaxial);
PSZ TTL Models	. . . . .1 slot, 2 TTL clock and data (2 BNC coaxial);
DCZ Differential Models	. . . . .1 slot, 1 RS-422 / LVDS clock and data (2 triax)
DSZ Differential Models	. . . . .1 slot, 1 RS-422 / LVDS clock and data (4 triax)
PSZ Differential Models	. . . . .1 slot, 1 RS-422 / LVDS clock and data (2 triax)
Maximum per Chassis	. . . . .32 (550) / 16 (Avalon)
Power	. . . . .5V @ 1 A; 3.3V @ 1 A
Environment	. . . . .See Base 550 System Chassis (PRO550B), Avalon System Chassis (AVALON-R), VME Mezzanine Carrier (ZCM596), and VME Mezzanine Carrier with Arbiter (ZCA596), data sheets
Dimensions	. . . . .75mm x 150mm (PMC standard)
Status Display	. . . . .10 LEDs

## Compatibility

VME Mezzanine Carrier (ZCM596)
VME Mezzanine Carrier with Arbiter (ZCA596)
Vista Software (Version 3.2.1 or higher)

## Ordering Information

DCZ543	. . . . .Decommutator, PMC (30 Mbps)
DCZ543-D	. . . . .Decommutator, PMC (30 Mbps), Differential
DCZ545	. . . . .Decommutator, PMC (50 Mbps)
DCZ545-D	. . . . .Decommutator, PMC (50 Mbps), Differential
DSZ543	. . . . .Decommutator / Simulator, PMC (30 Mbps)
DSZ543-D	. . . . .Decommutator / Simulator, PMC (30 Mbps), Differential
DSZ545	. . . . .Decommutator / Simulator, PMC (50 Mbps)
DSZ545-D	. . . . .Decommutator / Simulator, PMC (50 Mbps), Differential
PSZ543	. . . . .PCM Simulator, PMC (30 Mbps)
PSZ543-D	. . . . .PCM Simulator, PMC (30 Mbps), Differential
PSZ545	. . . . .PCM Simulator, PMC (50 Mbps)
PSZ545-D	. . . . .PCM Simulator, PMC (50 Mbps), Differential

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